23GHz Front-end Circuits in SiGe BiCMOS Technology

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Abstract – **This paper reports a monolithic 23GHz low-noise converter (LNC) and its blocks implemented in a commercial SiGe BiCMOS process featuring 70GHz f_t and 90GHz f_{max}. In general, measurement and simulation show close correspondence. For low-noise amplifier, 4.3dB noise figure (NF) and 22dB gain are typically obtained. For mixers, 13.5-15.5dB single sideband NF, 2-6dB gain and 2-8dBm IIP3 are measured, depending on whether or not linearizer is applied. The LNC converts an RF signal around 23GHz down to an IF of 1GHz. Its performance is described and related questions are discussed at the end of this paper.**

I. INTRODUCTION

SiGe heterojunction bipolar transistor (HBT) and BiCMOS technologies have developed aggressively in recent years, pushing f_T and f_{max} to 100GHz and above in production and well beyond 200GHz in research. This development offers an optional technology for applications in high-speed optical (≥ 40Gbps) and high-frequency microwave (≥20GHz) communications.

In commercial microwave radio applications, 23GHz is a well-utilized frequency band for wireless links. Implementation of SiGe technology into radio production may reduce the radio cost considerably as compared with using GaAs technology. This paper reports a 23GHz low-noise converter (LNC) and its block circuits which have been designed and manufactured in STMicroelectronics' 0.25μm SiGe BiCMOS process. The SiGe HBT in use has 0.4μm emitter width (drawn size), featuring 70GHz f_T and 90GHz f_{max} [1]. The process offers 5 metal layers for interconnects, MIM capacitors of 2fF/μm^2 and various types of resistors and inductors, all scalable.

The LNC circuit includes a low-noise amplifier (LNA) and a mixer. Simulation was carried out in ADS environment using both small signal and Harmonic Balance analysis. ADS built-in transmission line models were used for modeling of long RF paths. Paracitic extraction based on circuit layout has not been carried out in the design, which may results in effects not always negligible.

II. CIRCUITS AND THEIR PERFORMANCE

A. Low-Noise Amplifier

A 23GHz SiGe LNA has been designed earlier in a different process [2]. While noise figure and gain obtained in [2] are very similar to the results to be reported here, linearity was not under consideration there. Through out this work, particularly in mixer design, much of the design effort has been devoted to improving IIP3, input-referred third-order intercept point.

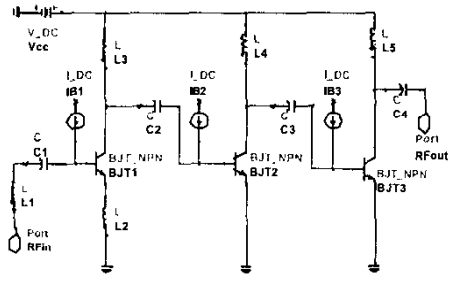

Fig. 1 LNA schematic

Fig.1 shows the LNA topology. It consists of three cascaded common-emitter stages. Inductive emitter degeneration is applied to the first stage to improve linearity and to help realizing simultaneous power and noise matching at LNA input port. Inductors are also

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used as collector load to reduce noise figure. Biasing is determined such that the first stage is optimized for low noise and the succeeding two stages for high gain. The LNA has a layout size of 0.7x0.6 mm^2 and consumes 26mA at a single 2.5V supplier.

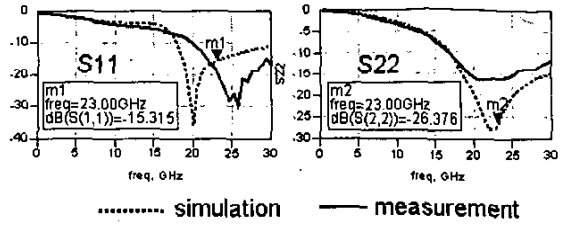

Fig. 2 S_{11} and S_{22}: measurement and simulation, 50Ω-referred

Measured S_{11} and S_{22} are shown in Fig.2 and are compared with simulated data. Less than –15dB return loss is obtained both in measurement and simulation. Although the S_{11} minimum shows a shift in frequency, the characteristic behavior is well reproduced by simulation over the whole frequency range. Re-simulation including parasitic extraction may explain the frequency shift in minimum S_{11} (work under progress). The reverse isolation, S_{12} (not shown here), is better than 50dB at 23 GHz.

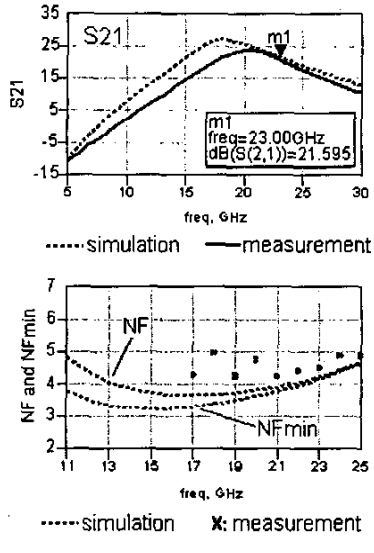

Fig. 3 Transducer power gain (upper) and noise figure (including simulated minimum noise figure, NFmin)

Fig.3 shows the small signal gain and noise figure, all 50Ω-referred. Again measurement and simulation demonstrate good correspondence, particularly around 23GHz. It should be noted that the LNA design in this work uses a narrow-band approach. Matching and optimization are only guaranteed for frequencies around 23GHz. In the design, the transducer gain at 23GHz is almost equal to the maximum available gain (not shown in Fig.3) and the noise figure is almost equal to the minimum noise figure. Therefore, simultaneous power and noise matching has been realized at the LNA input for 23GHz.

Totally four LNA samples are characterized and typical measured results are 4.3dB for NF and 22dB for gain. The oscillatory behavior seen in the mesured NF from 17 to 20GHz is caused by calibration. The LNA has an input 1dB-compression point of –15.4 dBm, same as simulated. The IIP3 is determined to be –6.2 dBm using 2-tone measurement, which is about 4dB lower than what is expected from simulation. Table I summarizes the LNA performance and compares measurement with simulation.

TABLE I. SUMMARY OF SIMULATED AND MEASURED LNA RESULTS

LNA @2.5V 23 GHz	Gain dB	NF dB	P1dB dBm	IIP3 dBm
Simulation	21.7	4.2	-15.0	-2.0
Measurement	21.5	4.3	-15.4	-6.2

B. Mixers

Double balanced Gilbert mixer (see Fig.4) is applied which converts 23GHz RF to 1GHz IF. This type of mixer topology may provide high conversion gain, moderate noise figure and high port-to-port isolation, but normally its linearity is relatively poor. In this design both inductive and resistive degeneration are utilized to the trans-conductance stage for linearity improvement.

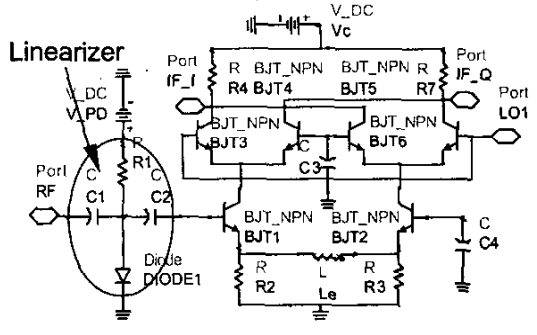

Fig. 4 Mixer and linearizer schematics

To further improve the linearity, a linearizer [3] is placed prior to RF input of the mixer. The linearizer is ac-coupled with the mixer and consists simply of a diode and a bias resistor. The diode is a nonlinear source, which compensates to some extent the nonlinearity generated by the mixer itself, and thus, reduces the nonlinear distortion of the whole circuit. However, because of its insertion loss the linearizer normally reduces conversion gain and increase noise figure as compared with Gilbert mixer without linearizer.

As for the LNA, two-tone measurement is carried out to determine IIP3 for the mixers. In Fig. 5 the IF output power and the power of 3rd order inter-modulation (IM3) product are plotted versus RF input power. Mixer with linearizer exhibits 6dB improvement in IIP3 over the pure Gilbert mixer. Corresponding simulated powers are also given in the figure. Satisfactory correspondence between simulation and measured is observed, although in general simulation overestimates slightly the IM3 power and thus, underestimates the IIP3. It should be pointed out that high IIP3 may also be obtained under high current consumption, hence high NF, instead of utilizing linearizer [4].

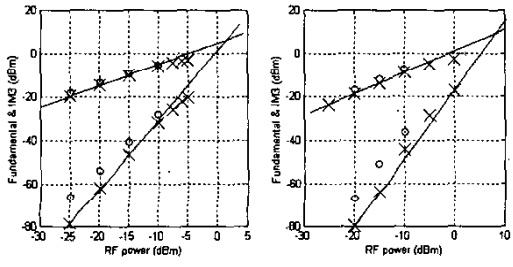

Fig. 5 Fundamental and IM3 power vs. RF input power for Gilbert mixer (left) and Gilbert mixer with linearizer (right); x: measured; o: simulated.

Fig. 6 plots the conversion gain and IIP3 as function of LO (local oscillator) power. Although the detailed values of the measured and simulated data do not exactly match, the general as well as the detailed features are well reproduced by simulation. Note that the lonearizer improves IIP3 by 6dB at LO power of 2.5dBm, with a cost of 4dB loss in conversion gain. It is therefore recommended to use when linearity is a more crucial parameter than conversion gain, which is the case here.

Fig.7 shows the single sideband (SSB) noise figure vs. LO power. 2dB-degradation in noise performance is caused by adding the linearizer.

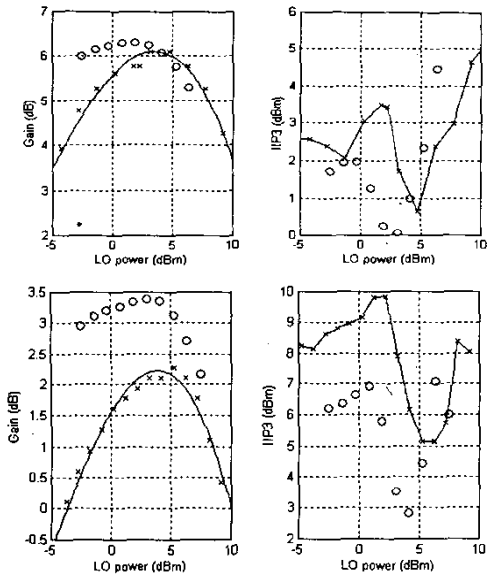

Fig.6 Conversion gain and IIP3 vs. LO power for Gilbert mixer (upper panel) and Gilbert mixer with linearizer (lower panel); x: measured; o: simulated

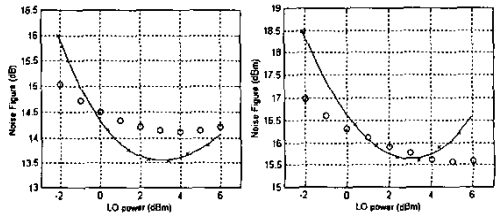

Fig. 7 Noise figure (SSB) vs LO power for Gilbert mixer (left) and Gilbert mixer with linearizer (right); x: measured; o: simulated

The mixer is 0.55x0.77 mm^2 in size and consumes 140-mW dc power at 3.9 volt. Table II summarizes mixer performance, including simulated and measured results.

TABLE II. SUMMARY OF SIMULATED AND MEASURED MIXER RESULTS

P_{LO}=2.5 dBm V_{cc}=3.9V	Mixer		Mixer with linearizer	
	Meas.	Sim.	Meas.	Sim
Gain (dB)	6.0	6.3	2.1	3.4
IIP3 (dBm)	2.0	0.2	8.0	5.8
NF (dB)	13.6	14.1	15.6	15.8

C. Integrated Low-Noise Converter (LNC)

A photograph of the monolithic LNC is shown in Fig.8. The real die size is 1.1x0.8 mm^2.

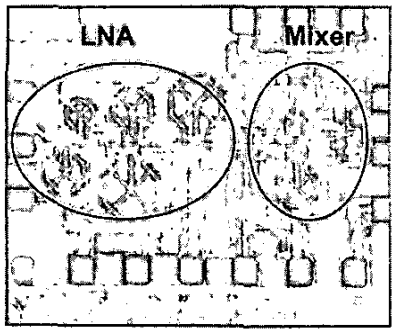

Fig. 8 Die photograph of the LNC

The conversion gain of the LNC without linearizer being applied to the mixer is measured to be 27.5dB. This is almost identical to the sum of LNA gain and mixer conversion gain, indicating that impedance match between the two is perfectly acceptable for power. The LNC IIP3 is measured as −19.5dBm, again almost identical to the value obtained by using equation: $(IIP3_{LNC})^{-1} = (IIP3_{LNA})^{-1} + G_{LNA}\,(IIP3_{Mixer})^{-1}$

The simulated double sideband (DSB) noise figure is 4.5dB which is consistent with prediction using Friis formula: $NF_{LNC} = NF_{LNA} + (NF_{Mixer}-1)/G_{LNA}$. The simulated SSB NF is 9.2 dB. This nearly 5dB-difference between DSB and SSB (normally 3dB) is caused by large gain-imbalance at the signal and image bands. Therefore, under proper image-rejection the LNC noise figure is expected to be about 4.5dB.

However, the measured DSB NF, ~7.5dB (see Table III), does not agree with simulation. Additional measurement and further investigation are required to understand the 3dB difference in noise figure. Coupling between LNA and mixer through substrate, for example, can be one of the reasons for the high noise figure obtained in measurement.

TABLE III. LNC PERFORMANCE

LNC	Gain dB	DSB-NF dB	SSB-NF dB	IIP3 dBm
Simulated	28.0	4.5	9.2	-20.0
Measured	27.5	~7.5	--	-19.5

It should be pointed out that a 24GHz integrated receiver front-end in SiGe HBTs has been reported early [5]. The LNA and mixer performance in [5] is not comparable with what is presented here, since the technology used in [5] was less advanced than the one used in present work.

III. CONCLUSIONS

A low-noise amplifier, active mixers and a single chip low-noise converter have been designed for 23 GHz operation and fabricated in a commercially available SiGe BiCMOS process. In general measurement and simulation agree well, implying that the models are sufficiently accurate for design at 20 GHz and above. The results reported here meet most of the requirements for microwave radio applications. This provides further motivation for SiGe to be used as an optional technology in high frequency, analog applications.

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